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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|------------------------|-------------|----------------------|---------------------|-------------------------|
| 10/653,234 | 09/03/2003 | Bin Yu | H1491 | 4829 |
| 45114 | 7590 | 08/26/2005 | EXAMINER | |
| HARRITY & SNYDER, LLP | | | NGUYEN, DAO H | |
| 11240 WAPLES MILL ROAD | | | | |
| SUITE 300 | | | ART UNIT | PAPER NUMBER |
| FAIRFAX, VA 22030 | | | 2818 | |
| | | | | DATE MAILED: 08/26/2005 |

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|------------------------|------------------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 10/653,234 | YU ET AL. <i>[Signature]</i> | |
| | Examiner | Art Unit | |
| | Dao H. Nguyen | 2818 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 05 July 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,2,4-6 and 15-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-2, 4-6, and 15-19 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All
 - b) Some *
 - c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date: _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. In response to the communications dated 07/05/2005, claims 1-2, 4-6, and 15-19 are active in this application.

Claim(s) 3 and 7-14 have been cancelled.

New claim(s) 19 has been added.

Remarks

2. Applicant's arguments filed 07/05/2005 have been carefully considered, but are moot in view of the new ground of rejections.

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim(s) 1-2, 4-6, and 15-19 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,927,130 to Suzuki, in view of Yu, U.S. Patent No. 6,395,589.

Regarding claim 1, Suzuki discloses a semiconductor device, as shown in figs. 2(A-J); comprising:

an ion implanted layer 4 (col. 1, lines 57-59);
a semiconductor layer 13 formed on the ion implanted layer 4, the semiconductor layer including a fin portion (under gate structure G) corresponding to a channel of the semiconductor device;
a source region S formed at a first end of the semiconductor layer 30, a height of the source region S being higher than that of the fin;
a drain region D formed at a second end of the semiconductor layer 13, a height of the drain region D being higher than that of the fin;
a metal gate region G formed to overlap at a top surface and at least one side surface of the fin; and
oxide sidewalls 21 formed adjacent to the metal gate region G and above the top surface of the fin. See also col. 7, line 3 to col. 8, line 60.

Suzuki does not necessarily teach that ion implanted layer 4 is an insulator layer. Nevertheless, it is well known in the art that layer 4 is a channel cut layer, or a layer to reduce leakage current or punch-through from the source/drain to the substrate (see further U.S. Patent No. 6,835,988 to Yamashita, col. 1, lines 51-60; col. 2, lines 51-58). It is also well known that insulators are great materials to form leakage current block.

Yu discloses a semiconductor device, as shown in figs. 2 and 17, comprising a gate structure formed between source/drain regions, and a buried insulating layer 132 (fig. 2) or 202 (fig. 17) formed under the gate and source/drain regions.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Suzuki to replace the ion implanted layer 4 by an insulating layer as that of Yu to enhance the control of the electrical characteristics of the device (see col. 2, lines 9-17 of Yu), also to obtain a device with less cost since forming an oxide buried layer is much easier and cheaper than forming a buried ion implanted layer.

Regarding claim 2, Suzuki/Yu discloses the device wherein the metal gate region G overlaps the top surface and two side surfaces of the fin. See fig. 2J of Suzuki.

Regarding claim 4, Suzuki/Yu discloses the device wherein the source S and drain D regions are silicided (see col. 7, lines 52-58; col. 8, lines 19-22. Note that, technically, an annealing process applied to the source/drain regions will result in obtaining silicided source/drain regions).

Regarding claim 5, Suzuki/Yu discloses the device comprising all claimed limitations, except for explicitly teaching that a distance between the insulator and the

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metal gate region is about 500 Å to about 700 Å and a distance between the insulator and a top of the source or the drain region is about 600 Å to about 1000 Å.

However, it would have been obvious to one of ordinary skill in the art that such distances in the device of Suzuki/Yu can be varied depending on the desired properties of the device and the application of the device, since such a varying/modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

Regarding claim 6, Suzuki/Yu discloses the device wherein the metal gate comprises at least one of tungsten, titanium, nickel, TaSiN, and TaN. See col. 7, lines 43-47; col. 8, lines 48-54 of Suzuki.

Regarding claim 15, Suzuki discloses a semiconductor device, as shown in figs. 2(A-J), comprising:

an ion implanted layer 4 (col. 1, lines 57-59);

a semiconductor layer 13 formed on the ion implanted layer 4, the semiconductor layer including a fin portion (under gate structure G) corresponding to a channel of the semiconductor device;

a source region S formed from a first end of the semiconductor layer 30, a height of the source region S being higher than that of the fin;

a drain region D formed from a second end of the semiconductor layer 13, a height of the drain region D being higher than that of the fin; a metal gate region G formed to overlap at a top surface and at least one side surface of the fin: and sidewall spacers 21 formed adjacent at least portion of the metal gate region G.

See also col. 7, line 3 to col. 8, line 60.

Suzuki does not necessarily teach that ion implanted layer 4 is an insulator layer. Nevertheless, it is well known in the art that layer 4 is a channel cut layer, or a layer to reduce leakage current or punch-through from the source/drain to the substrate (see further U.S. Patent No. 6,835,988 to Yamashita, col. 1, lines 51-60; col. 2, lines 51-58). It is also well known that insulators are great materials to form leakage current block.

Yu discloses a semiconductor device, as shown in figs. 2 and 17, comprising a gate structure formed between source/drain regions, and a buried insulating layer 132 (fig. 2) or 202 (fig. 17) formed under the gate and source/drain regions.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Suzuki to replace the ion implanted layer 4 by an insulating layer as that of Yu to enhance the control of the electrical characteristics of the device (see col. 2, lines 9-17 of Yu), also to obtain a

device with less cost since forming an oxide buried layer is much easier and cheaper than forming a buried ion implanted layer.

Moreover, Suzuki does not necessarily teach that a width of the source region being wider than that of the fin, and a width of the drain region being wider than that of the fin.

However, it would have been obvious to one of ordinary skill in the art that the size of the source and the drain regions in the device of Suzuki/Yu can be varied depending on the desired properties of the device and the application of the device; and that a modification to vary such size would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

Regarding claim 16, Suzuki/Yu discloses the device wherein the sidewall spacers have a width ranging from about 150 Å to about 1000 Å. See col. 8, lines 5-9.

Regarding claim 17, Suzuki/Yu discloses the device, wherein the source and drain regions are silicided. See col. 7, lines 52-58; col. 8, lines 19-22. Note that, technically, an annealing process applied to the source/drain regions will result in obtaining silicided source/drain regions.

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Regarding claim 18 Suzuki/Yu discloses the device comprising all claimed limitations, except for explicitly teaching that a thickness of the fin portion ranges from about 500 Å to about 700 Å and a thickness of the source and drain regions range from about 600 Å to about 1000 Å.

However, it would have been obvious to one of ordinary skill in the art that such thicknesses in the device of Suzuki/Yu can be varied depending on the desired properties of the device and the application of the device, since such a varying/modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

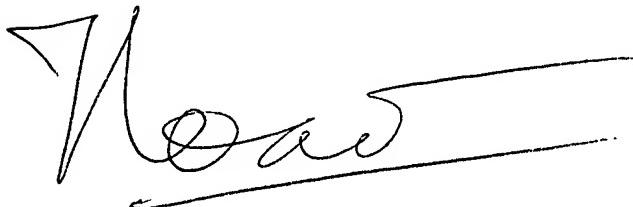
Regarding claim 19, Suzuki/Yu discloses the semiconductor device wherein the sidewall spacers have a width ranging from about 150 Å to about 1000 Å. See col. 8, lines 5-9.

Conclusion

5. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.



Dao H. Nguyen
Art Unit 2818
August 24, 2005



David Nelms
Supervisory Patent Examiner
Technology Center 2800